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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. MIYAMOTO et al

Serial No.

Filed: April 28, 2000

For: SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING THE SAME

**PRELIMINARY AMENDMENT**

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to the examination thereof, please amend the above-identified patent application as follows.

**IN THE CLAIMS**

Please amend claims 22, 25 and 26 and add new claims 30 - 33 as follows.

22. (Amended) A semiconductor device manufacturing process as set forth in claim 20 [or 21], further comprising:

dicing and dividing the chip areas of said semiconductor wafer into semiconductor chips.

25. (Amended) A semiconductor device manufacturing process as set forth in claim 20 [or 21], further comprising:

forming slits in the principal face or back face of said semiconductor wafer at the boundary of said chip areas, and forming protective layers in said slits.

26. (Amended) A process for manufacturing a semiconductor device, comprising:

(a) forming a plurality of semiconductor elements and a plurality of bonding pads over the individual principal planes of a plurality of chip areas of the semiconductor wafer defined by scribe lines;

(b) forming an elastomer layer over the principal faces of said plurality of chip areas;

(c) forming through holes ins aid elastomer layer at positions, as corresponding to said plurality of bonding pads, individually in said plurality of chip areas;

(d) forming such conductive layers individually in said plurality of chip areas which are formed at their one-end portions over said elastomer layer and connected at their other end portions with the corresponding ones of said bonding pads through said through holes;

(e) forming bump electrodes individually in said plurality of chip areas which are connected with the one-end portions of said conductive layers; and

(f) cutting said semiconductor wafer along said scribe lines to form over its principal face a plurality of semiconductor chips having said elastomer layers, said conductive layers and said bump electrodes.

--30. A semiconductor device comprising: a semiconductor wafer having a plurality of semiconductor chip forming areas defined by scribe lines and having a plurality of semiconductor elements and a plurality of bonding pads formed on the principal faces thereof; an elastic insulating film formed on the principal faces of said semiconductor chip forming areas and having through holes at positions corresponding to said plurality of bonding pads;

a plurality of conductive layers having their one-end portions thereof formed on said insulating film while the other end portions thereof are electrically connected to said plurality of bonding pads corresponding thereto through said through holes; and a plurality of bump electrodes formed on the one-end portions of said plurality of conductive layers and electrically connected to said plurality of bonding pads corresponding thereto through said conductive layers.--

--31. A semiconductor device as set forth in claim 30, characterized in that a plurality of semiconductor chips are supplied by cutting said semiconductor wafer along said scribe lines.--

--32. A semiconductor device as set forth in claim 30, characterized in that said conductive layer includes the Au bump electrodes individually formed on the surfaces of said

plurality of bonding pads and wiring layer formed over said Au bump electrodes.--

#33 cont'd

--33. A semiconductor device as set forth in claim 30, characterized in that said bump electrodes are solder bump electrodes, respectively.--

**REMARKS**

Examination is requested.

Respectfully submitted,

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